HIGH-SPEED, CURRENT-DRIVEN LATCH

Abstract of the Invention

A high-speed, current-driven latch is provided. The latch conducts a current and includes an output, a SET circuit and a RESET circuit. The output is variable between a first state and a second state. The SET circuit conducts the current present in the latch at the first state such that the SET circuit is maintained close to a level required to change the output of the transistor from the first to the second level, and the RESET circuit conducts the current at the second level such that the RESET circuit is close to a level required to change the output of the transistor from the second level to the first level.